Science and Engineering Research Board (SERB) funded High-End Workshop
on
VLSI Architectures for Signal and Image Processing (VASIP-2022)
(17th - 23rd December, 2022)

About the Department:

The Department of Electronics Engineering came into existence as an offshoot of Electrical Engineering Department in the year 1971 with a great effort from Prof. S.S. Banerjee. In the same year the erstwhile Banaras Engineering College (BENCO), College of Mining and Metallurgy and College of Technology were amalgamated to form the Institute of Technology-Banaras Hindu University (IT-BHU). Our current priority areas of specialization are (i) Communication Systems Engineering (ii) Digital Techniques & Instrumentation (iii) Microwave Engineering and (iv) Microelectronics.

Objective and Scope:

Lots of novel algorithms are published in the multidisciplinary research areas of signal and image processing. Most of the work is based on simulations performed using higher level languages like MATLAB, C, C++, OpenCV, Python etc. and it is executed on sophisticated computers. Consequently, all these algorithms cannot be executed in real time and are unsuitable for real applications. So, only few of these algorithms are modeled on hardware platform over the period of time.

Hardware Description Languages (HDLs), Verilog and VHDL, play vital role while translating these algorithms for real time applications. During this phase an algorithm must translated, synthesized and mapped on to a given technology. Additionally, one has to fulfill the area, speed and power constraint requirements of the design. This is possible when one has very good understanding of digital circuit design. Therefore, VLSI architectures for various algorithms in signal and image processing domain will be introduced in this high-end workshop. So, the objectives of this course are:

- To introduce some of the important algorithms used in signal and image processing
- Understanding hardware perspective like design optimization, resource sharing and parallel-pipelining etc.
- Thinking in terms of Digital Design
- Translating algorithms to VLSI Architectures
- Understanding low power VLSI Design strategies
- Understanding the role of timing constraints and design closure

About the KARYASHALA:

KARYASHALA scheme by SERB is meant for skill development training on topics required for scientific research work. It is an effort to improve research productivity of promising PG and PhD students from universities and colleges through high-end workshops on specific themes. This program aims to provide opportunities to acquire specialized research skills.

Who can attend:

The workshop is open to postgraduate students/research scholars from all Institutes and Universities. Preference will be given to the students having interest towards Digital VLSI Design, Embedded Systems, HDL – Verilog, FPGA implementation.

- Permission letter duly signed by the competent authority is essential to attend the workshop.
- **There is no registration fees.**
- **Total number of seats is limited to 25.**
- Students selected for this workshop are eligible for Travel allowance (TA) reimbursement for their journey to IIT (BHU) Varanasi from their host institute as per SERB and GoI norms.
- Accommodation to the participants will be provided at IIT (BHU), Varanasi Guest house/hostel with catering facilities.
- A certificate of participation would be issued to all participants.

Resource Persons Confirmed:

- Dr. Deepak Mishra, ISRO-SAC, Ahmadabad
- Dr. Debapriya Basu Roy, Department of CSE, IIT Kanpur
- Dr. K.C. Ray, Department of EE, IIT Patna
- Prof. Ekram Khan, Department of ECE, AMU
- Dr. Pradyut Biswal, Department of E & TC, IIIT Bhubaneswar
- Dr. Praful Pai, Mathworks India

Important dates:

Registration Opens: **15th November, 2022**

Registration Closes: **30th November, 2022**

Registration Confirmation through email: **2nd December, 2022**

Workshop Dates: **17 - 23 December, 2022**

Registration link:

https://forms.gle/goFCE9Xhr5puKoh9A

Contact for Queries
Email: skishor.ece@iitbhu.ac.in
Izhar Khan **Cell No:** (+91) 81719 33667
Bharat Bhushan **Cell No:** (+91) 90262 64226

Workshop Coordinator
Dr. Kishor P. Sarawadekar
Department of Electronics Engineering
IIT (BHU), Varanasi-221 005