PROJECT ON

DESIGN AND DEVELOPMENT OF
A SMART ENERGY GRID ARCHITECTURE WITH ENERGY STORAGE
DST- SERI SPONSORED PROJECT (No. GP/LT/EE/2015-16/03)
Department of Electrical Engineering
Indian Institute of Technology (BHU), Varanasi-221 05

Draft Advertisement for putting on IIT (BHU), Varanasi webpage

Applications are invited for the post of Senior Research Fellow (2Nos.) for the Project of DST-SERI titled "Design **and Development of a Smart Energy Grid Architecture with Energy Storage**", Ministry of Science & Technology, Department of Science & Technology, Government of India for the **period of 3 years**. The SRFs appointed may pursue the Ph. D. under the Project Investigator in the above area if found suitable for doctoral research. *The post is purely temporary and coterminous with Project.*

Qualification:

Essential: (1) The candidates must have first class B. Tech. in Electrical Engineering / M. Tech. in Power Systems with institute of repute.

(2) The candidate must be conversant with advance technology of Smart Grid & Intelligent Control preferably with 2 years of relevant experience.

(3) GATE qualified, **Upper Age Limit 32 years**

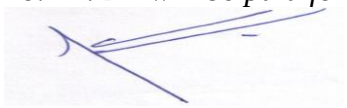
Desirable: The candidate having broad base of power systems and advance control with software applications and algorithmic development shall be preferred.

A relaxation of five years in age will be given to SC/ST, physically handicapped, female candidates. All things being equal, SC/ST candidates will be preferred as per GOI rules.

Fellowship Amount: ***The SRF will be paid as per notification SR/S9/Z-09/2012 dated Oct. 21, 2014 of DST, Ministry of Science and Technology, Govt. of India.*** The present fellowship is Rs. 28000.00 + 20% HRA at Varanasi and other facilities will be the same as in notification.

Application on plain paper with full academic/experience details along with necessary supporting documents and address for communication & email must reach to Prof. R. K. Pandey, Principal Investigator of DST-SERI Project, Department of Electrical Engineering, Power Systems Complex, Indian Institute of Technology (BHU), Varanasi-221 005 by June 15, 2015 positively.

No. TA/DA will be paid for attending interview.



(Prof. R. K. Pandey)
Principal Investigator, DST-SERI Project
Design and Development of a Smart Energy Grid Architecture with Energy Storage
Department of Electrical Engineering,
Indian Institute of Technology (BHU), Varanasi-221 005